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09/855,594	05/16/2001	Toyohiko Yoshida	57454-116	9350

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EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 08/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/855,594	YOSHIDA ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 15-19* is/are pending in the application.

4a) Of the above claim(s) *14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 15-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05/16/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-13,15-19 are presented for examination. Claim 14 has been canceled.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-13 and 15-18 rejected under 35 U.S.C. 103(a) as being unpatentable over Okado (EP 0511484 A2) in view of Hennessy (Computer Architecture).

3. As to claim 1 , Okado taught a data processing system comprising at least :

a) an instruction memory in which an instruction is stored (see figure 1, [201]), Column 9, lines 4-8 show that this ROM is a program or instruction memory.

b) a data memory in which data is stored (figure 1 , element 101).,

c) an instruction decoder decoding a fetched instruction (figure 1, I D E C) ;

d) a memory operation unit (figure 1, elements 103 and 207) connected to said instruction memory, said data memory and said instruction decoder, fetching an instruction stored in said instruction memory, and accessing said data memory according to a decode result of said instruction decoder', (Column 10, lines 12-15 show that the repeat controller portion allows instructions to be read (fetched) from the micro ROM (instruction memory). Okado's Figure 1 showed a pointer portion is used to access the data memory based on the decoder output on line 202.) and an integer

operation unit carrying out an integer operation based on a result of an instruction decoder, Figure 1 shows ALU 1 , which performs arithmetic functions and is an integer unit. The outputs 204 of the decoder. Column 9, lines 28-31 showed that this output of the decoder controls the arithmetic logic operations.)

4. Okado did not disclose the instruction memory including a plurality of instruction memory banks, and the memory operation unit generating a pipeline cycle corresponding to selection of an instruction memory bank and a pipeline cycle corresponding to instruction readout from said selected instruction memory bank to carry out pipeline processing when a plurality of instructions are fetched from a plurality of said instruction memory banks. However, Hennessy disclosed the use of memory banks for memory systems (e.g. see in pages 361-363) . Page 362 shows that one memory bank initiation or read is completed per clock cycle. It showed that when reading from multiple banks, one bank is read from while the other is then selected in a generated cycle so that in the next generated cycle that bank is read from. This selection must take place before fetching can occur and is inherently during a clock cycle. This cycle may be the same cycle as the transfer is made from the selected bank or it may be in a prior cycle, however in any case a pipeline cycle is generated that corresponds to the selection of the memory bank.

5. In addition, Hennessy shows that multiple memory banks allow for producing or accepting one word fetched or stored per clock cycle, which is faster than using one memory bank (see Page 361). The faster speed of memory transfers would have

motivated one of ordinary skill in the art to use multiple memory banks (as taught by Hennessy) in the instruction memory. It would have been obvious to one of ordinary skill in the art at the time of invention to use Hennessy into Okado with modified configuration parameters (e.g. the R/W port) to include a plurality of memory banks in the instruction memory system of Okado in order to increase the throughputs of the transfer operation of the memory, and therefore, provided a motivation.

6. As to the claim language : "without reading out any instruction from unselected instruction banks" (see claim 1, line 14), Hennessy taught when reading from multiple banks, one bank was read from while the other was then selected in a generated cycle (e.g. see page 362). It can be seen clearly that the selection of memory bank was at the generated current cycle, not the next cycle, therefore, no reading of instruction was performed from the unselected bank in the given cycle because the reading of instruction was only applicable into the selected bank in a given cycle.

7. As to claim 2, Okado did not explicitly show the first bank select circuit decoding an address including a low order address to generate chip select signals of said plurality of instruction memory banks so that a different instruction memory bank of said plurality of instruction memory banks is accessed when instructions at continuous addresses are accessed. However, It is most likely that if two instructions are stored at two memory addresses separated by the border of memory banks, that the memory bank must be switched to access the second instruction and that the low order address

would play a role in chip-selecting the bank since it gives the border address of the bank.

8. As to claim 3, Okado did not disclose the instruction memory further includes a high speed instruction memory, wherein said memory operation unit generates a pipeline cycle corresponding to instruction readout to carry out a pipeline process when fetching an instruction from said high speed instruction memory.

However, Hennessy disclosed the operation of caches in the memory Hierarchy (see pages 18-20). The cache does not have memory banks and thus does not require a cycle to select a bank. A cache is a fast or high-speed memory. Furthermore, Hennessy disclosed that a cache is a fast or high-speed Local memory for holding commonly used information. A fast memory to fetch instructions faster would have motivated one of ordinary skill in the art to modify Okado in to include an instruction cache. Therefore, It would have been obvious to one of ordinary skill in the art at the time of invention to include a cache for the reasons set forth above.

9. As to claim 4, Okado did not specifically disclose the data memory when accessing said plurality of data memory banks. However, Hennessy disclosed the use of memory banks for memory systems(e.g. see pages 361-363) . It shows that one memory bank initiation or read is completed per clock cycle , and that when reading from multiple banks, one bank is read from while the other is then selected in a generated cycle so that in the next generated cycle that bank is read from (Page 362) . Hennessy also showed multiple memory banks allow for producing or accepting one word fetched or stored per clock cycle, which is faster than using one memory bank (

Page 361) . The faster memory transfers would have motivated one of ordinary skill in the art to modify Okado to use multiple memory banks in the data memory.
It would have been obvious to one of ordinary skill in the art at the time of invention to use Okado with Hennessy to include a plurality of memory banks in the data memory system as taught by Hennessy so that transfers of the memory could be enhanced.

10. As to claim 5, Okado did not explicitly show the data processing apparatus according to claim 4, wherein said data memory further includes a second bank select circuit decoding an address including a high order address to generate chip select signals of said plurality of data memory banks in order to divide said plurality of data memory banks into two different regions. However, It is most likely that a higher order address will divide a memory bank into two sections. The highest bit of a memory address that switches within a memory bank indicates two section of that memory bank.

11. As to claim 6, Okado did not specifically show the second bank select circuit decodes an address including a low order address to generate chip select signals of said plurality of data memory banks so that a different data memory bank in said plurality of data memory banks is accessed when data at continuous addresses in the two different areas are accessed. However, it is most likely that if two instructions are stored at two memory addresses separated by the border of memory banks, that the memory bank must be switched to access the second instruction and that the low order

address would play a role in chip-selecting the bank since it gives the border address of the memory bank.

12. As to claim 7, Okado did not disclose wherein said data memory generates a pipeline cycle corresponding to data access to carry out a pipeline process when accessing said high speed data memory. However, Hennessy disclosed caches in the memory hierarchy (pages 18-20). The cache did not have memory banks and therefore did not require a cycle to select a bank. A cache is a fast or high-speed memory. Hennessy showed that a cache is a fast or high-speed Local memory for holding commonly used information. The ability to have a fast memory to retrieve data from would have motivated one of ordinary skill in the art to use Okado in view of Hennessy as applied above to include a data cache. It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Okado in view of Hennessy as applied to above to include a cache as taught by Hennessy for storing instructions so that data could be retrieved faster.

13. As o claim 8, Okado in view of Hennessy disclosed a memory operation unit fetches an instruction from said instruction memory via an instruction bus (Okado, figure 1, 201 to IR1) and accesses said data memory via a data bus (figure 1, Page 9 [106]) differing from said instruction bus.

14. As to claim 9, Okado also included a memory operation unit that reads out data from the data memory via a data input bus, and writes data into said data memory via a data output bus differing from said .data input bus. Okado disclosed a bus that inputs data to the data memory and a separate bus that outputs data from the data memory (e.g. see fig.1)

15. As to claim 10, Okado disclosed an instruction memory in which an instruction is stored (figure 1, 201, Col. 9, lines 4-8 , see the ROM); a data memory in which data is stored (figure 1, 101); an instruction decoder decoding a fetched instruction (figure 1 , I D E C); a register file (figure 1 , IRI and IR2); a memory operation unit (figure 1, elements 103 and 207) connected to the instruction memory, said data memory and said instruction decoder, fetching an instruction stored in said instruction memory, and accessing said data memory according to a decoded result of said instruction decoder', col. 10, lines 12-15 show that the repeat controller portion allows instructions to be read (fetched) from the micro ROM (instruction memory). Figure 1 shows that the a the pointer portion is used to access the data memory based on the decoder output on line 202.) and an integer operation unit carrying out an integer operation according to a decoded result of said instruction (see fig.1 ALU) which performed arithmetic functions and is an integer unit. Notice the outputs 204 of the decoder. Col.9, lines 28-31, see the output of the decoder controls the arithmetic logic operations.), the memory operation unit retaining, in a register in said register file, an instruction in a loop of instructions corresponding to a repeat instruction in a dedicated register in said register file when said repeat instruction is executed, and executing the loop of instructions

while fetching the instruction retained in said dedicated register. (Col. 9, line 35 - column 10, lines 48, see the repeat controller was part of the memory operation unit) , stored one or more repeat instructions in instruction registers so that when executing a repeat loop the instructions are fetched from the registers instead of memory. Since no specific dedication of the register ahs been reflected into the claim, the register is read as a register for storing data.

16. Okado did not teach the memory operation unit generates a pipeline cycle corresponding to selection of an instruction memory bank and a pipeline cycle corresponding to instruction readout from said selected instruction memory bank to carry out pipeline processing when a plurality of instructions are fetched from a plurality of said instruction memory banks. Okado disclosed one memory bank initiation or read is completed per clock cycle (Page 362). However, Hennessy disclosed the use of memory banks (e.g. see pages 361-363). It showed the reading from multiple banks, and one bank was read from while the other then selected in a generated cycle so that in the next generated cycle that bank is read from. The selected bank must be performed before fetching could begin and was most likely in a given cycle. There, a pipeline cycle is generated that corresponds to the selection of the memory bank. Okado also taught producing or accepting one word fetched or stored per clock cycle (Page 361). Hennessy disclosed multiple memory banks for faster access than memory bank. The faster memory transfers would have motivated one of ordinary skill in the art to use Okado to include multiple memory banks in the instruction

memory. It would have been obvious to one of ordinary skill in the art at the time of invention to use Okado to include a plurality of memory banks in the instruction memory system as taught by Hennessy so that transfers of the memory could be increased.

17. As to claim 11, Okado disclosed register file comprises a processor status word. The word at a first execution cycle of said loop, and retains, in the register of said register file, the instruction in the loop of instructions fetched from said instruction wherein said memory operation unit sets a flag in said processor status memory when said repeat instruction is executed', (As shown above, on first execution of a loop, instructions of the loop are retained in the registers IRI and IR2 after fetching from memory. This section showed the repeat controller had an internal state (status flag) to cause fetching from memory or the registers. So when the fetching is done from the memory, the processor status flag is set to do so. The processor status flag was a processor status word. Okado also taught a cycle of said loop, and executed the loop while fetching the instruction retained and included reset flag in the processor status word at a second execution in the dedicated register. The fetching was done from the registers, the processor status word is reset or set to fetch from these registers.

18. As to claim 12, Okado in view of Hennessy discloses the data processing apparatus according to claim 10, wherein said memory operation unit retains a plurality of instructions in the loop of instructions in a plurality of dedicated registers in said

register file when said repeat instruction, and executes said loop of instructions while fetching said plurality of instructions retained in said plurality of dedicated registers (see Col.10, lines 33-48, see the plurality of instructions repeated and fetched from a plurality of registers. The register is read as register for storing data.

19. As to claim 13, Okado in view of Hennessy discloses the data processing apparatus according to claim 12, wherein said register file includes a processor status word, and wherein said memory operation unit sets a flag in said processor status word at a first execution cycle of said loop, and retains the plurality of instructions in the loop of instructions fetched from said instruction memory in said plurality of registers, and resets said flag in said processor status word at a second execution cycle of said loop, and executes said loop while fetching said plurality of instructions retained in said plurality of dedicated registers. From the above, the multiple instructions could be retained and the processor status word (i.e. the flags) could be used to fetch instructions from memory and upon doing so and retaining them for future fetching from the registers, the status was reset.

20. As to claim 15, Okado also disclosed the instruction memory further comprises a first bank select circuit decoding an address including a low order address to generate chip select signals of said plurality of instruction memory banks so that a different instruction memory bank of said plurality of instruction memory banks is accessed when

instructions at continuous addresses are accessed. It is most likely that if two instructions are stored at two memory addresses separated by the border of memory banks, the memory bank must be switched to access the second instruction and that the low order address would play a role in chip-selecting the bank since it gives the border address of the bank.)

21. As to claim 16, Okado did not disclose the data memory included a plurality of data memory banks, wherein the memory operation unit generated a pipeline cycle corresponding to selection of a data memory bank . However, Hennessy disclosed the use of memory banks for memory systems (pages 361-363). It showed one memory bank initiation or read was completed per clock cycle (see Page 362). It showed when reading from multiple banks, one bank was read from while the other is then selected in a generated cycle so that in the next generated cycle that bank was read from.

22. Hennessy also disclosed multiple memory banks for producing or accepting one word fetched or stored per clock cycle (see page 361), which was faster than memory bank. This memory transfer speed would have motivated one of ordinary skill in the art to use of Okado in view of Hennessy to include multiple memory banks in the data memory. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use Okado in view of Hennessy to include a plurality of memory banks in the data memory system as taught by Hennessy in order tom increase the transfers speed of the memory.

23. As to claim 17, Okado also included a second bank select circuit decoding an address including a high order address to generate chip select signals of said plurality

of data memory banks in order to divide said plurality of data memory banks into two different regions. It is most likely that a higher order address will divide a memory bank into two sections. The highest bit of a memory address that switched within a memory bank indicates two section of that bank memory.

24. As to claim 18, Okado also included a low order address to generate a chip select signal of said plurality of data memory banks so that a different data memory bank in said plurality of data memory banks is accessed when data at continuous addresses in said two different regions are accessed. (It is most likely that if two instructions are stored at two memory addresses separated by the border of memory banks, that the memory bank must be switched to access the second instruction and that the low order address would play a role in chip-selecting the bank since it gave the memory bank border address.

25. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okado in view of Hennessy and Watanabe (5,214,786).

26. As to claim 19, neither Okado nor Hennessy specifically disclosed the memory operation unit saves a plurality of registers including said dedicated register and switches a task in a task switch operation as claimed. Watanabe disclosed in the abstract that registers are selectively saved on a task switch, and the saving registers on a task switch, critical information was stored so a switch back. The abstract as well as the Summary then showed that by the selection immediately and the saving portion is done faster. This ability to save critical information quickly would have motivated one

of ordinary skill in the ad at the time of invention to modify the design of Okado in view of Hennessy to include register saving on task switches as taught by Watanabe. It would have been obvious to one of ordinary skill in the art at the time of invention to Watanabe in Okado to include the register saving technique on a task switch in order to provide a faster save of the critical system conditions .

27. Furthermore, Hennessy also disclosed a different bank was fetched from or one transfer was made each clock cycle (see pages 362 - 363) . The examiner holds that in order to fetch from a different memory bank each cycle, the bank must be selected before the transfer can begin. The selection must take place during a clock cycle. This cycle could be the same cycle as the transfer was made from the selected bank or it could be in a prior cycle. Nevertheless, a pipeline cycle was generated corresponding to the selection of the memory bank.

28.

29. Okado (EP 0511484 A2) , Watanabe (5,214,786) and Hennessy (Computer Architecture) were cited to applicant in a previous action , therefore, copies are not being provided herein.

30. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Mochizuki et al. (5,483,497) is cited for the teaching of the bank selection only if the readout instruction was activated (col.6, lines 5-11).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

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